REMARKS

The present application was filed on February 20, 2002 with claims 1 through 20. Claims 1 through 20 are presently pending in the above-identified patent application. Claims 5, 11, 14, and 19 are proposed to be amended herein.

In the Office Action, the Examiner rejected claims 1-20 under 35 U.S.C. §112, second paragraph, as being incomplete for omitting essential elements and rejected claims 1-6 and 16-20 under 35 U.S.C. §101 because the claimed invention is directed to non-statutory subject matter. The Examiner also rejected claims 1-2, 5, 7-8, 11, 13-14, 16, and 19 under 35 U.S.C. §102(e) as being anticipated by Kikuchi (United States Patent Number 6,606,715), rejected claims 3, 9, and 17 under 35 U.S.C. §103(a) as being unpatentable over Kikuchi in view of Hwu et al. (United States Patent Number 6,681,387), and rejected claims 4, 6, 10, 12, 15, 18, and 20 under 35 U.S.C. §103(a) as being unpatentable over Kikuchi in view of Borg et al. (United States Patent Number 5,274,811).

The specification has been amended to correct a typographical error.

Section 112 Rejections

Claims 1-20 were rejected under 35 U.S.C. §112, second paragraph, as being incomplete for omitting essential elements. Regarding claims 1, 7, 13, and 16, the Examiner asserts that there is no connection or relationship made between establishing a bound due to task interference to anything else in the body of the claim. Regarding claims 5, 11, 14, and 19, the Examiner asserts there is insufficient antecedent basis for the limitation "the sets."

Contrary to the Examiner's assertion, the cited claims require the limitation of establishing the bound based on the number of live frames and, thus, there is a connection between the preamble (establishing a bound on the execution time of an application due to task interference in an instruction cache shared by a plurality of tasks) and the body of the claims. Claims 5, 11, 14, and 19 have also been amended to correct the antecedent basis for the cited limitation. Applicants therefore respectfully request that the rejection of the cited claims under 35 U.S.C. § 112, second paragraph, be withdrawn.

Section 101 Rejections

Claims 1-6 and 16-20 were rejected under 35 U.S.C. §101 because the claimed invention is directed to non-statutory subject matter. In particular, the Examiner asserts that the cited claims are not tangibly embodied in a manner so as to be executable.

The Supreme Court has stated that the "[t]ransformation and reduction of an article 'to a different state or thing' is the clue to patentability of a process claim." *Gottshalk v. Benson*, 409 U.S. 63, 70, 175 U.S.P.Q. (BNA) 676 (1972). In other words, claims that require some kind of transformation of subject matter, which has been held to include intangible subject matter, such as data or signals, that are representative of or constitute physical activity or objects have been held to comply with Section 101. *See, for example, In re Warmerdam,* 31 U.S.P.Q.2d (BNA) 1754, 1759 n.5 (Fed. Cir. 1994) or *In re Schrader*, 22 F.3d 290, 295, 30 U.S.P.Q.2d (BNA) 1455, 1459 n.12 (Fed. Cir. 1994).

Thus, as expressly set forth in each of the independent claims, the claimed methods or system describe a method for establishing a bound on the execution time of an application due to task interference in a shared instruction cache and transform the number of live frames in a cache to a bound on the execution time. The steps of determining a number of live frames of said application that are coexistent during execution of said application; and establishing said bound based on said number of live frames required by the independent claims of the present disclosure include all the essential steps of establishing the cited bound. This transformation to a bound on the execution time provides a useful, concrete and tangible result.

Applicants submit that each of the claims 1-20 are in full compliance with 35 U.S.C. §101, and accordingly, respectfully requests that the rejection under 35 U.S.C. §101 be withdrawn.

Independent Claims 1, 7, 13 and 16

Independent claims 1, 7, 13, and 16 were rejected under 35 U.S.C. §102(e) as being anticipated by Kikuchi. Regarding claim 1, the Examiner asserts that Kikuchi discloses determining a number (block count / boundary of data blocks) of live frames (blocks during execution) of said application that are coexistent during execution of said application (col. 11, lines 30-67); and establishing said bound based on said number of live frames (block count / boundary of data blocks) (col. 11, lines 30-67).

Applicants note that Kikuchi is directed to "a device control apparatus and a control method for forming protection data such as a CRC or the like and adding it when user data from an upper apparatus such as a host or the like is buffered into a cache memory." (Col. 1, lines 12-16). Applicants also note that Kikuchi teaches a case

> where the transfer is interrupted in association with the path switching of the fabric 12. In this state, the transfer of the data block and the formation of the protection data cannot be simultaneously performed. On the other hand, in the RAID controllers 18-1 to 18-3 of the invention, a fact that the *transfer of the data block was interrupted is detected during the transfer of the user data from the host and a state of the forming circuit of the protection data at that time is stored. After that, when the restart of the transfer of the data block is detected, the state is returned to the stored circuit state upon interruption and the formation of the protection data is restarted.*"
> (Col. 6, lines 47-59; emphasis added.)

Kikuchi, however, does ***not*** address the issue of establishing a bound on the execution time of an application due to task interference in a shared instruction cache, as required by the claims of the present invention.

Applicants also note that the present disclosure defines "live cache frames" as, for example, "a cache frame that contains a *block that is accessed in the future without an intervening eviction.* The present invention recognizes that the eviction of blocks from a live frame by an interrupt causes a future miss that would not otherwise occur and that evictions from live frames are the only evictions that cause misses that would not otherwise occur." (Page 2, lines 19-22; emphasis added.) Applicants could find no disclosure or suggestion by Kikuchi of live frames, of determining *a number of live frames* of said application that are *coexistent during execution* of said application; and of *establishing said bound based on said number of live frames.* Independent claims 1, 7, 13, and 16 require determining a number of live frames of said application that are coexistent during execution of said application; and establishing said bound based on said number of live frames.

Thus, Kikuchi does not disclose or suggest determining a number of live frames of said application that are coexistent during execution of said application; and establishing said bound based on said number of live frames, as required by independent claims 1, 7, 13, and 16.

Additional Cited References

Borg et al. was also cited by the Examiner for its disclosure of a cache simulation routine to analyze memory access patterns of a cache. Applicants note that Borg is directed to utilizing "link time code modification to instrument the code which is to be executed, typically comprising plurality of kernel operations and user programs." (See, Abstract.) Applicants could find no disclosure or suggestion by Borg et al. of live frames, of determining *a number of live*

frames of said application that are *coexistent during execution* of said application; and of *establishing said bound based on said number of live frames.*

Thus, Borg et al. do not disclose or suggest determining a number of live frames of said application that are coexistent during execution of said application; and establishing said bound based on said number of live frames, as required by independent claims 1, 7, 13, and 16.

Hwu et al. was also cited by the Examiner for its disclosure of detecting and monitoring usage patterns of the data elements in a cache line after access (col. 3, lines 27-54). Applicants note that Hwu is directed to detecting and monitoring program hot spots during execution that may be implemented in hardware. (See, Abstract.) Applicants could find no disclosure or suggestion by Hwu et al. of live frames, of determining *a number of live frames* of said application that are *coexistent during execution* of said application; and of *establishing said bound based on said number of live frames.*

Thus, Hwu et al. do not disclose or suggest determining a number of live frames of said application that are coexistent during execution of said application; and establishing said bound based on said number of live frames, as required by independent claims 1, 7, 13, and 16.

Dependent Claims 2-6, 8-12, 14-15 and 17-20

Dependent claims 2, 5, 8, 11, 14, and 19 were rejected under 35 U.S.C. §102(e) as being anticipated by Kikuchi, claims 3, 9, and 17 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kikuchi in view of Hwu et al., and claims 4, 6, 10, 12, 15, 18, and 20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kikuchi in view of Borg et al.

Claims 2-6, 8-12, 14-15, and 17-20 are dependent on claims 1, 7, 13, and 16, respectively, and are therefore patentably distinguished over Kikuchi, Hwu et al., and Borg et al., alone or in combination, because of their dependency from independent claims 1, 7, 13, and 16 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

All of the pending claims, i.e., claims 1-20, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

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Kevin M. Mason
Attorney for Applicants
Reg. No. 36,597
Ryan, Mason & Lewis, LLP
1300 Post Road, Suite 205
Fairfield, CT 06824
(203) 255-6560